

# Enabling Traditional Processor Architectures to Relay Non-Binary Information with Electronic Alfvén Wave Imposition and Readout via Precision Timing

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## Introduction

In the search for solutions to enable non-conventional computing, the prospect of being able to integrate precision timing mechanisms of reduced size, weight and power requirements featuring precision equal to or better than established atomic clocks is, in this author's opinion, certain to enable feats of computing not possible without such a capability. For example, this author has previously written about the possibility of storing large quantities of data optically within an optical carousel in which data can only be accessed by being able to predict the precise moment at which a pulse of light will complete a loop within an optical pathway and whereas the stored data is perpetually in-transit. This requires an atomic clock be integrated into the system. The following proposal, provided such an integrated and miniaturized atomic clock (one of which was invented by this author in 2022) is available, should be viable when coupled with the ingredient of a magnetism-gating superstrate capable of selectively introducing a magnetic field to the immediate area encompassing individual transistors on a case-by-case basis in order to encode additional layers of data.

## Abstract

In optics, a little-known phenomenon known as Alfvén waves are periods in a detected optical signal in which no photons (or ions, or electrons, depending upon context) exist due to the influence of a magnetic field. Photons and electrons will tend to bunch together, leaving gaps, provided that they either spend a substantial amount of time in a weak magnetic field (as in the case of light traveling from the Sun through the Earth's magnetic field) or, perhaps, a short period of time in a strong magnetic field.

The gaps are generally on the order of picoseconds and therefore can only be measured with precision with the aid of atomic timing.

Recent advancements in metamaterials allow for structures to be built capable of blocking magnetic fields which are only two or three atoms thick. Some of these materials can be tailored to permit magnetism to pass through the materials on the condition that the materials are electrified.

If we were to add to a conventional processor such a superstrate with a fixed source of magnetism on the other side of the barrier, we could impose Alfvén waves upon flowing current within a conventional computing architecture with only the need for modest modifications.

Minute areas in the conditionally permissive superstrate each of which correspond positionally to an individual transistor in the primary processing layer may be locally electrified to varying degrees depending upon how much

magnetism, if any, one wishes to permit through the layer. The greater the amount of the magnetism, the greater the number of Alfvén lines could be expected to be imposed upon the flowing current. In this way, a single pulse of electricity could be made to represent a great many more values than merely zero and one.

Although something similar might be achieved with memristors (without having to use precision timing to count Alfvén lines) memristors are substantially larger in size than transistors. With the aforementioned approach, however, a conventional transistor of much smaller size can be made to carry information beyond the values of zero and one whereas each subsequent transistor in a series presents a new opportunity for additional Alfvén lines to be added to the streaming electrons whereas the total number of lines can be counted at the end of each processing step provided the aforementioned precision timing capability. As mentioned in my publication concerning an entirely different type of unconventional processor I term a magristor processor, so long as only prime values are introduced and so long as each magnetic actuator is programmed to introduce different primes, the inputs can be deduced from the outputs.

## **Conclusion**

In theory, this would increase the processing capacity of any given chip by a minimum of a power of two as there would be an option to either Alfvénize the current or not at each transistor and there would be, furthermore, the potential for varying degrees of magnetism to be used to introduce entirely bespoke Alfvén characteristics at each possible juncture.

From here, the bottleneck would move to on-chip caches and, to a lesser extent, RAM and the ability to handle extremely large numbers in order to make best use of the capability. Such a capability would, however, be beneficial moreso for cryptological and cognitive tasks and less-so for those requiring large numbers of floating-point operations.